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Question Paper Code : 23462

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Sixth Semester

Electronics and Communication Engineering

EC 2354 — VLSI DESIGN

(Common to Biomedical Engineering)

(Regulations 2008)

(Also common to PTEC 2354 — VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering — Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Compare CMOS and BiCMOS technology.

2. Draw the DC transfer characteristics of CMOS inverter.

3. State the types of power dissipation.

4. Define Scaling. What are the advantages of scaling?

5. List the various power losses in CMOS circuits.

6. Enumerate the features of synchronizers.

7. What is need for testing VLSI circuits?

8. Define boundary scan test.

9. Write the Verilog module for a 1-bit full adder.

10. Give an example for implicit continuous assignment.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the different steps involved in n-well CMOS fabrication process with neat diagram. (10)

(ii) Draw the CMOS inverter and discuss its DC characteristics. Write the conditions for the different regions of operation. (6)

Or

(b) (i) An NMOS transistor has a nominal threshold voltage of 0.16V. Determine the shift in threshold voltage caused by body effect using the following data. The nMOS transistor is operating at a temperature of 300°K with the following parameters : gate oxide thickness $(t_{OX}) = 0.2 \times 10^{-5} cm$, relative permittivity of gate oxide $(\varepsilon_{OX}) = 3.9$, relative permittivity of silicon $(\varepsilon_{Si}) = 11.7$, substrate bias voltage = 2.5 V, intrinsic electron concentration $(Ni) = 1.5 \times 10^{10} / cm^3$, impurity concentration in substrate $(N_A) = 3 \times 10^{16} / cm^3$. Given Boltzmann's constant $= 1.38 \times 10^{-23} J / °K$, electron charge $= 1.6 \times 10^{-19}$ Coulomb and permittivity of free space $= 8.85 \times 10^{-14} F / cm$. (8)

(ii) Explain the principle of SOI technology with net diagrams. Discuss its advantages and disadvantages. (8)

12. (a) (i) Explain the power dissipation of static CMOS design in detail. (8)

(ii) Define Logical Effort and reason-out why mostly NAND gates are used to realize the combinational circuits rather than NOR gates. (4)

(iii) Discuss resistance and capacitance of a interconnect. (4)

Or

(b) (i) Explain the constant field scaling. Write its advantages. (8)

(ii) List out all device characterization and explain any two, (8)

13. (a) (i) Implement a XOR gate using CMOS logic. (8)

(ii) Compare CMOS, Dynamic, Domino and Pseudo nMOS logic families. (8)

Or

(b) (i) Design a d-latch using transmission gate. (8)

(ii) Design a 1-bit dynamic inverting and Non-inverting Register using pass transistor. (8)

14. (a) Explain the Design For Testability (DFT) concepts. (16)

Or

(b) Explain the following terms :

(i) Silicon debug principles (8)

(ii) Boundary scan technique. (8)

15. (a) Write a Verilog HDL for an 8-bit Ripple Carry Adder using structural model.

Or

(b) Write a Verilog HDL for a positive edge-triggered D-flip-flop. Using that implement an 8-bit shift register in structural model.
